1/12

FIG. 1

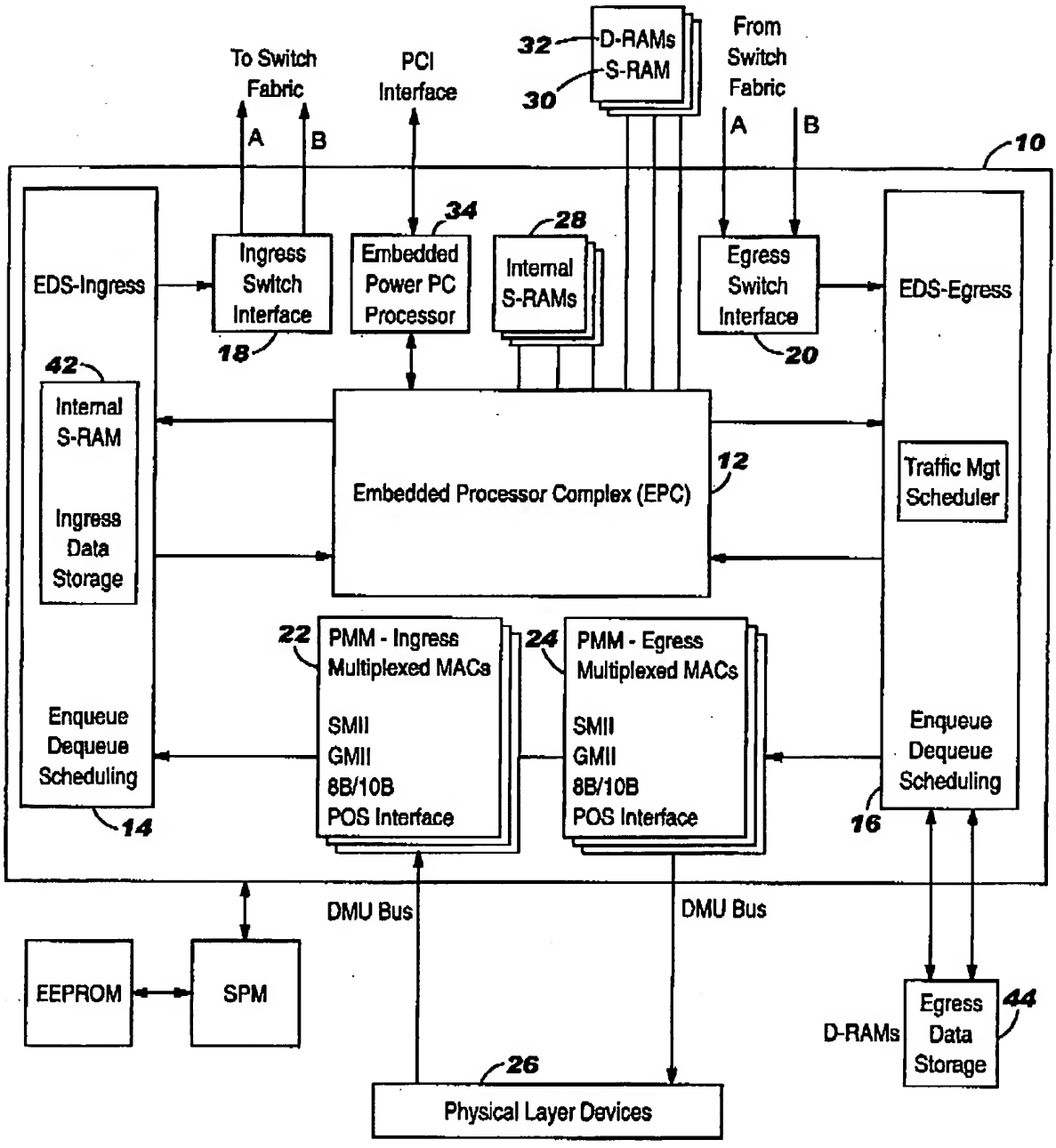

To Switch Fabric
A
B
PCI Interface
32
D-RAMs
S-RAM
30
From Switch Fabric
A
B
10
EDS-Ingress
Ingress Switch Interface
18
34
Embedded Power PC Processor
28
Internal S-RAMs
Egress Switch Interface
20
EDS-Egress
42
Internal S-RAM
Ingress Data Storage
Embedded Processor Complex (EPC)
12
Traffic Mgt Scheduler
22
PMM - Ingress Multiplexed MACs
SMII
GMII
8B/10B
POS Interface
24
PMM - Egress Multiplexed MACs
SMII
GMII
8B/10B
POS Interface
Enqueue Dequeue Scheduling
14
Enqueue Dequeue Scheduling
16
DMU Bus
DMU Bus
EEPROM
SPM
D-RAMs
Egress Data Storage
44
26
Physical Layer Devices

FIG. 2

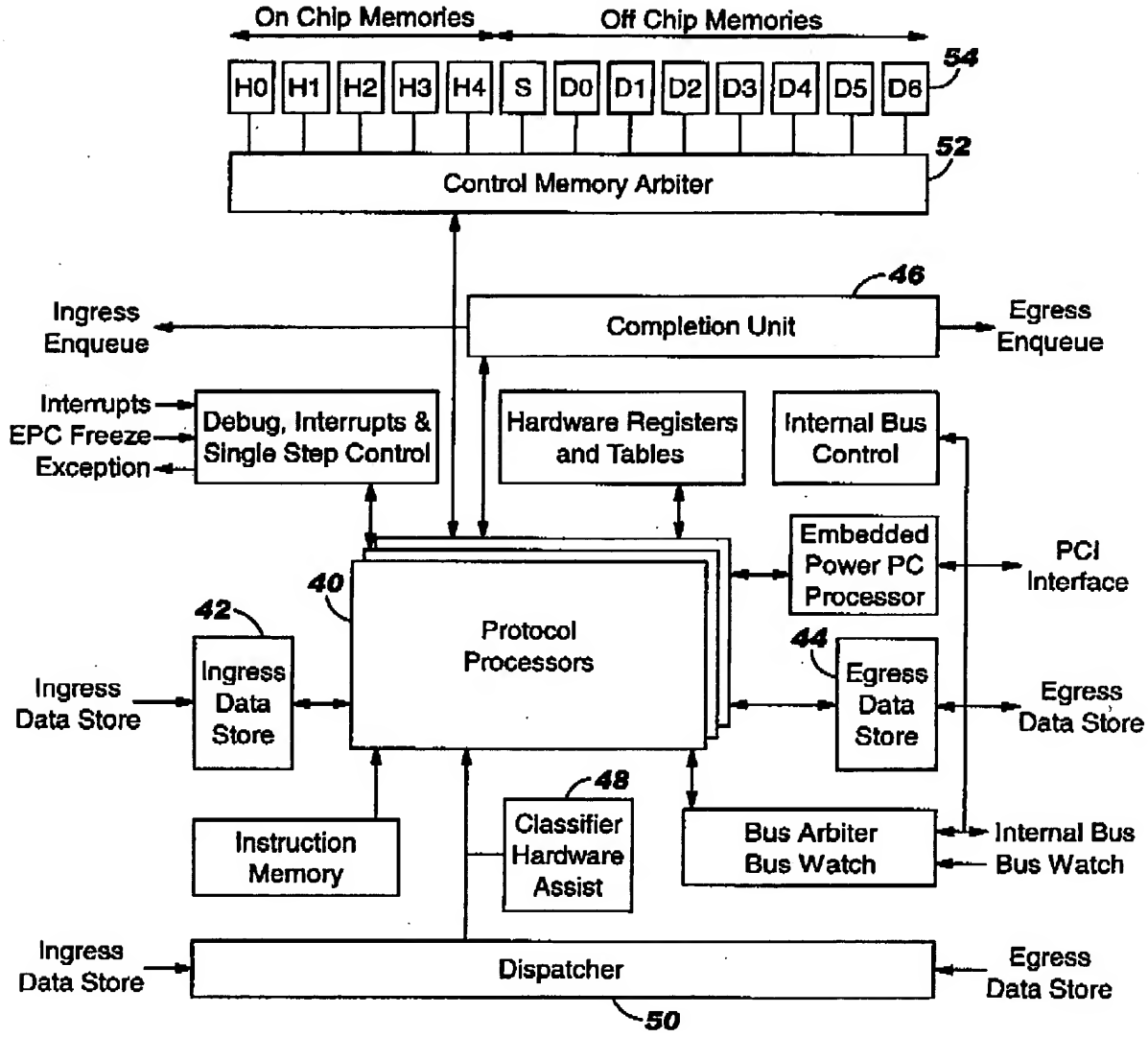

On Chip Memories
Off Chip Memories
H0
H1
H2
H3
H4
S
D0
D1
D2
D3
D4
D5
D6
54
Control Memory Arbiter
52
46
Ingress Enqueue
Completion Unit
Egress Enqueue
Interrupts
EPC Freeze
Exception
Debug, Interrupts & Single Step Control
Hardware Registers and Tables
Internal Bus Control
Embedded Power PC Processor
PCI Interface
40
Protocol Processors
42
Ingress Data Store
Ingress Data Store
44
Egress Data Store
Egress Data Store
48
Instruction Memory
Classifier Hardware Assist
Bus Arbiter Bus Watch
Internal Bus
Bus Watch
Ingress Data Store
Dispatcher
Egress Data Store
50

FIG. 3

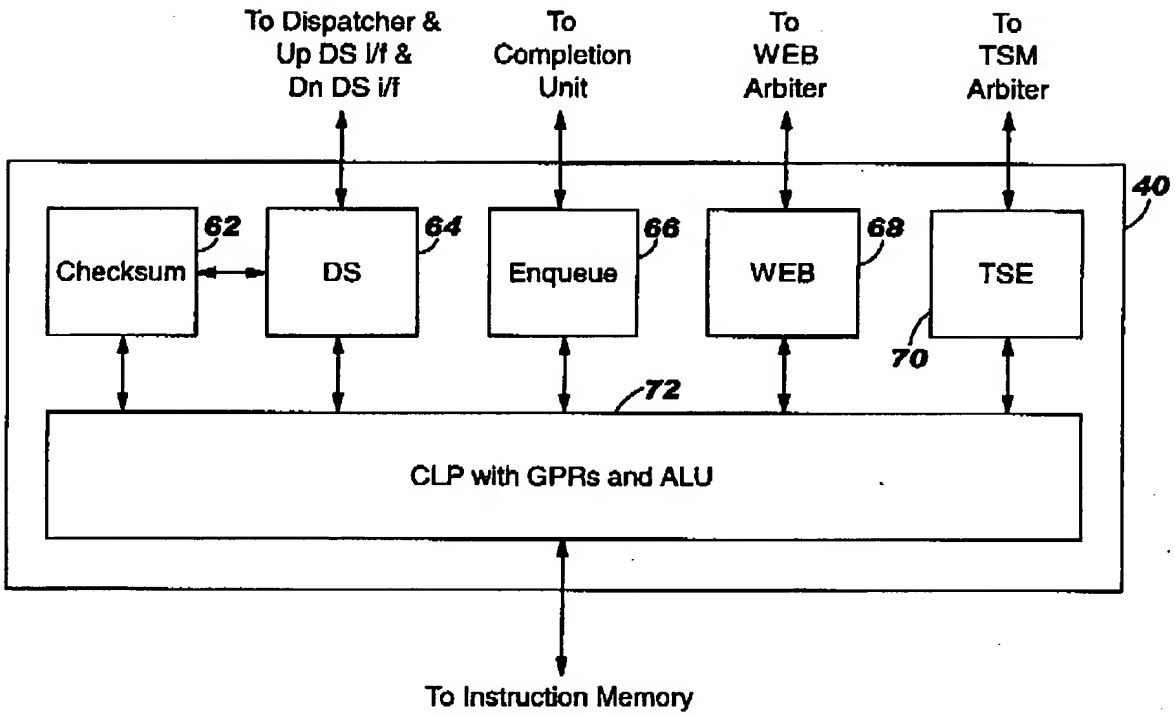

To Dispatcher & Up DS I/f & Dn DS i/f
To Completion Unit
To WEB Arbiter
To TSM Arbiter
40
Checksum
62
DS
64
Enqueue
66
WEB
68
TSE
70
72
CLP with GPRs and ALU
To Instruction Memory

FIG. 4

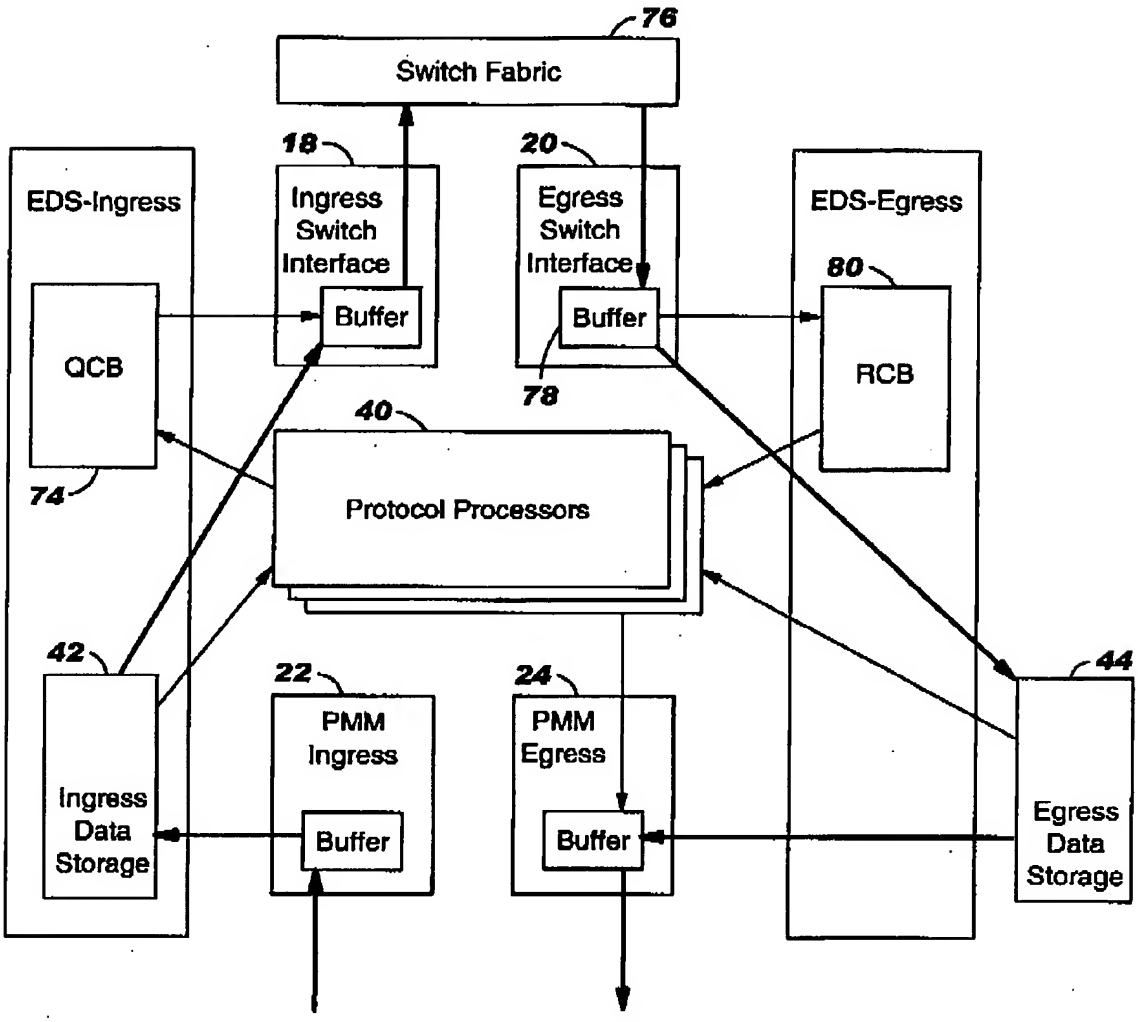
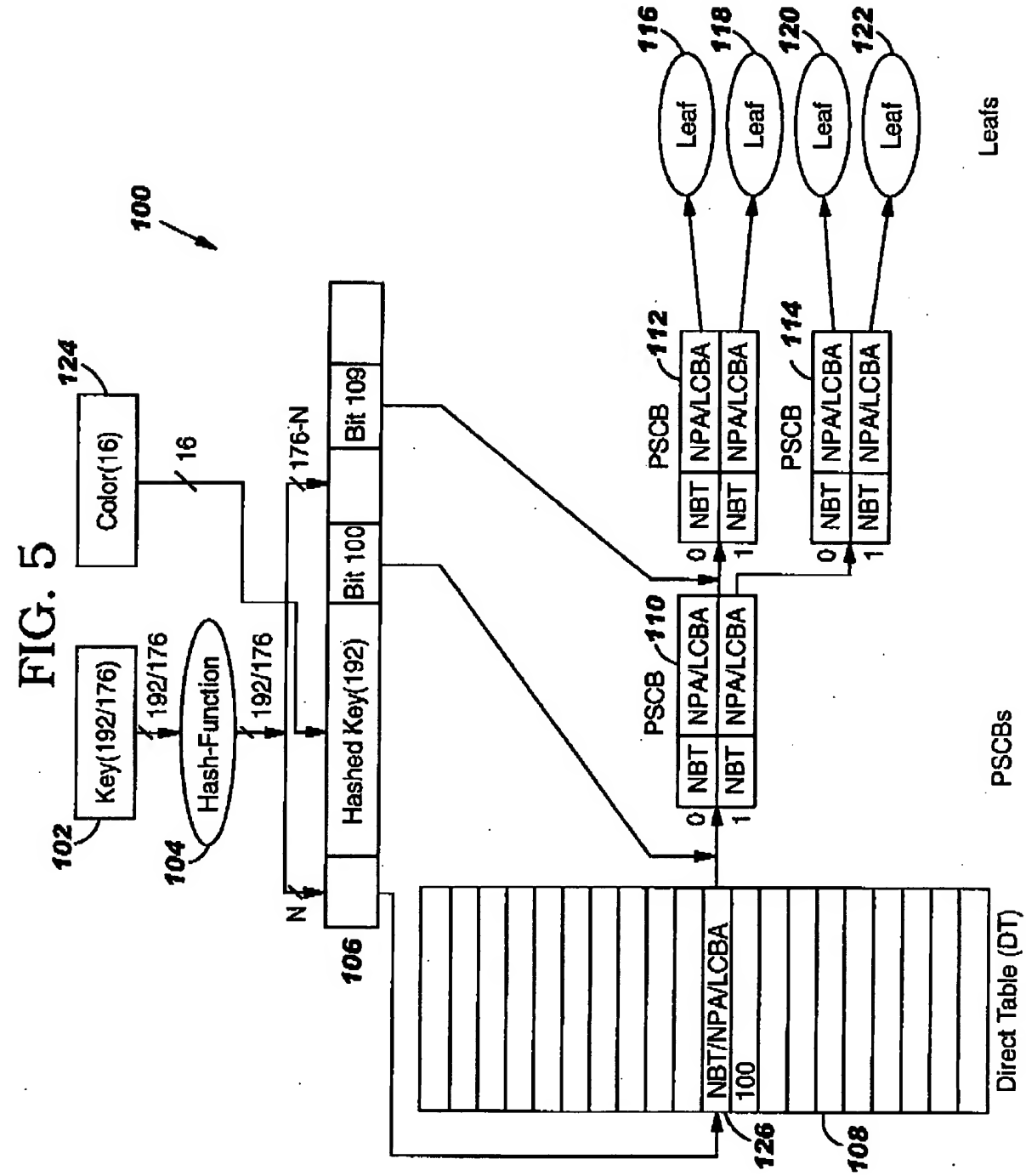

76
Switch Fabric
18
Ingress Switch Interface
Buffer
20
Egress Switch Interface
Buffer
78
EDS-Ingress
EDS-Egress
80
QCB
74
RCB
40
Protocol Processors
42
Ingress Data Storage
22
PMM Ingress
Buffer
24
PMM Egress
Buffer
44
Egress Data Storage

FIG. 5


100
102
Key(192/176)
104
Hash-Function
106
Hashed Key(192)
Bit 109
Bit 100
176-N
N
124
Color(16)
16
192/176
192/176
PSCB 110
PSCB 112
PSCB 114
NPA/LCBA
NBT
0
1
116
118
120
122
Leaf
Leafs
PSCBs
Direct Table (DT)
NBT/NPA/LCBA
100
126
108

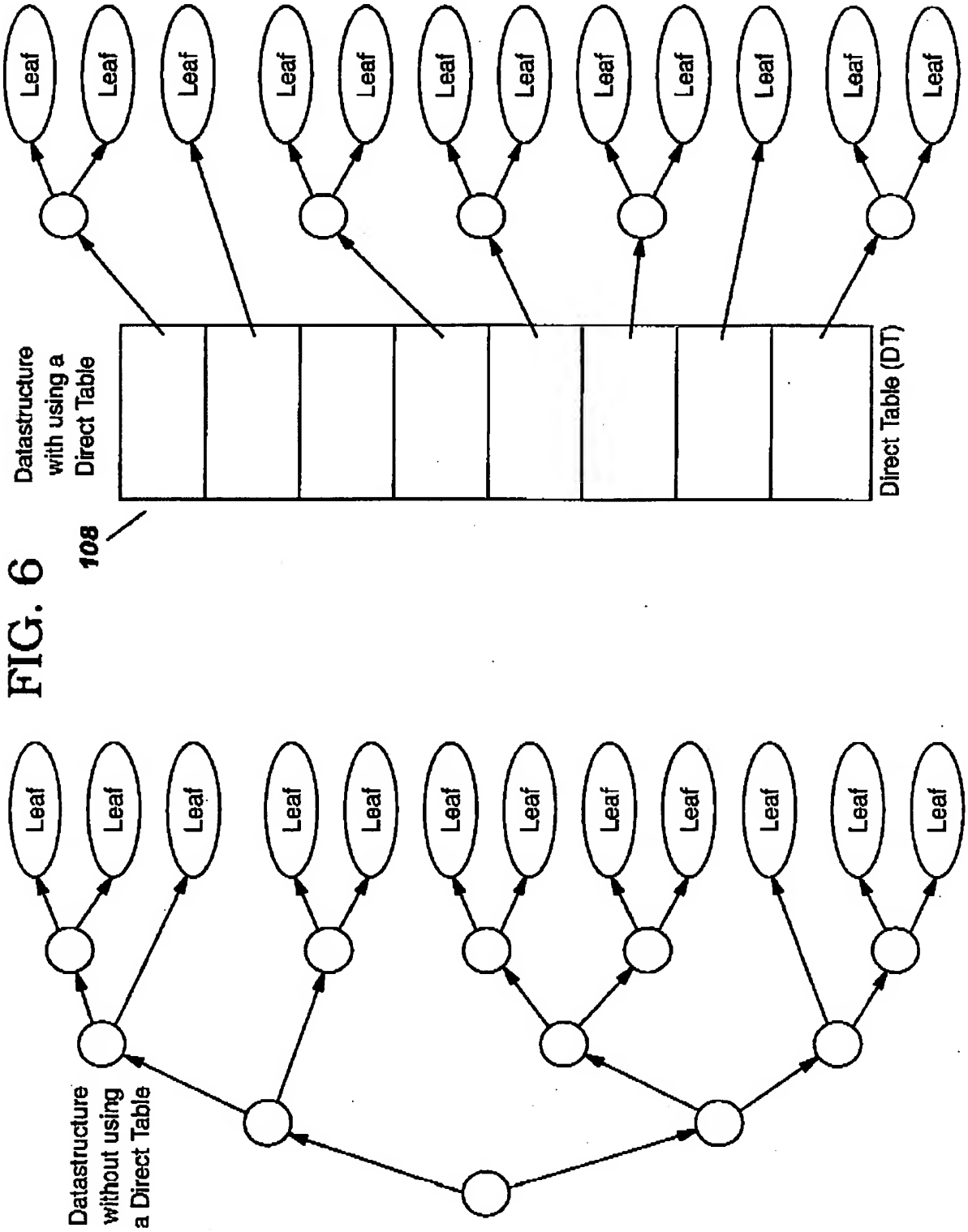

Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Datastructure with using a Direct Table
108
Direct Table (DT)
Datastructure without using a Direct Table

FIG. 6

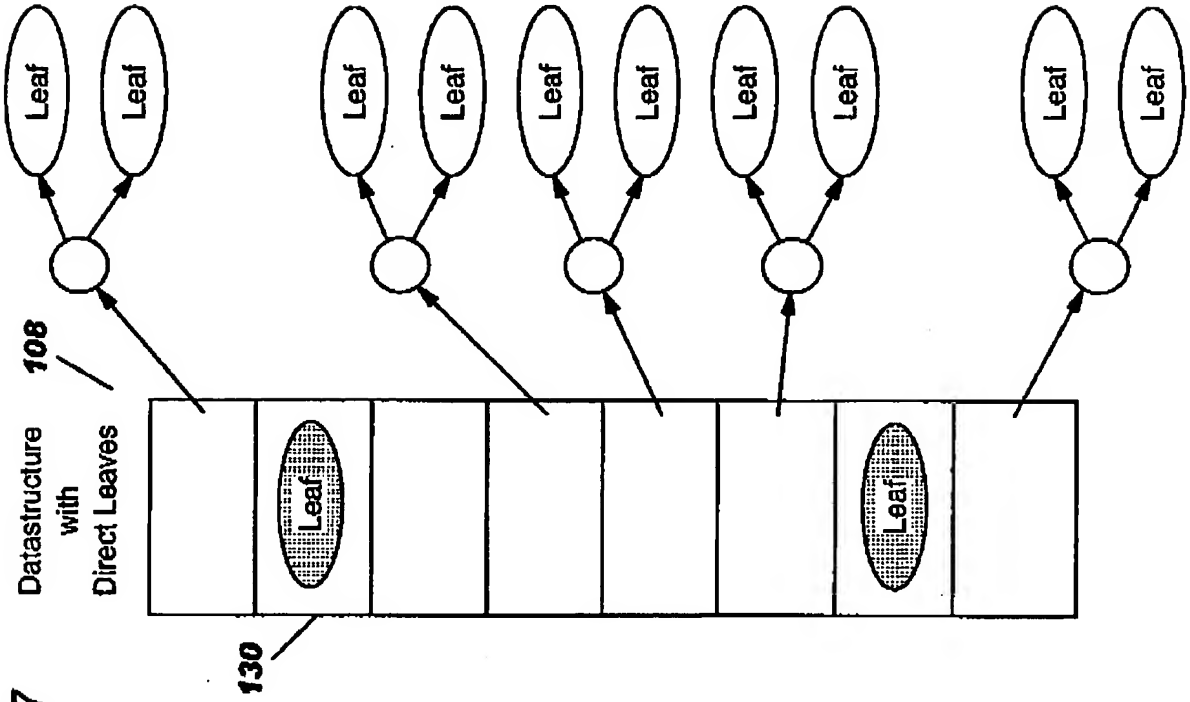

Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
108
Datastructure with Direct Leaves
Leaf
Leaf
130

FIG. 7

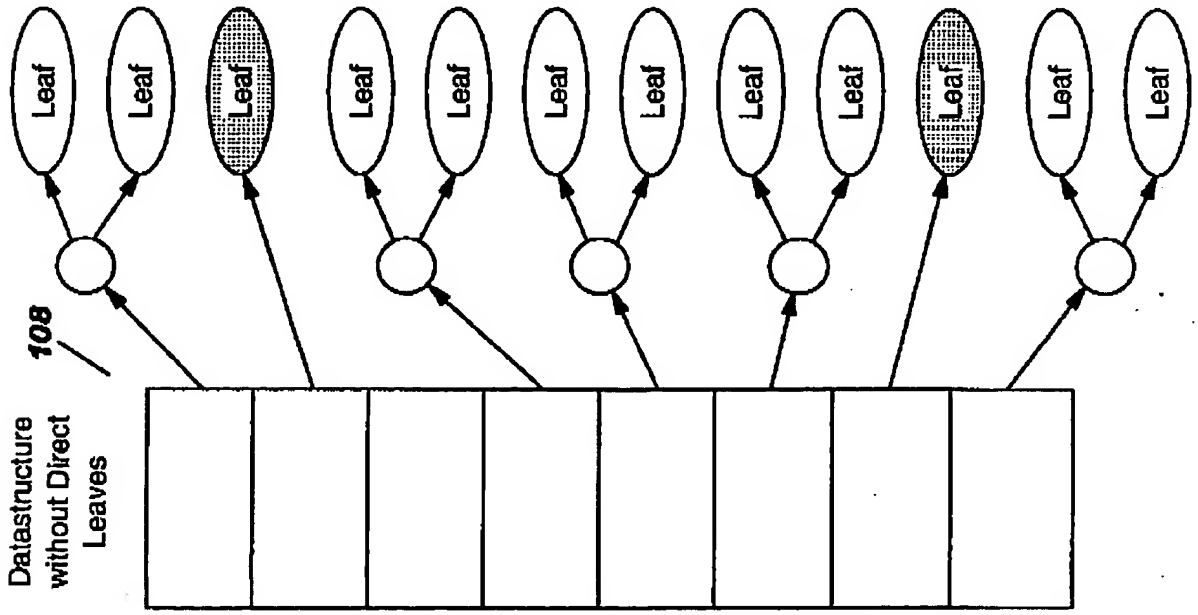

Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
Leaf
108
Datastructure without Direct Leaves

FIG. 8

Format	Conditions	Valid in DTEntry ?	Valid in PSCB?	Format (2bits)	NPA/LCBA (26 bits)	NBT (8 bits)
Empty DTEntry	No leaves	Yes	No	00	0	0
Pointer to next PSCB	DtEntry contains pointer	Yes	Yes	00	NPA	NBT
Pointer to leaf	Single leaf associated with DTEntry; LCBA field contains pointer	Yes	Yes	01	LCBA	0

FIG. 9

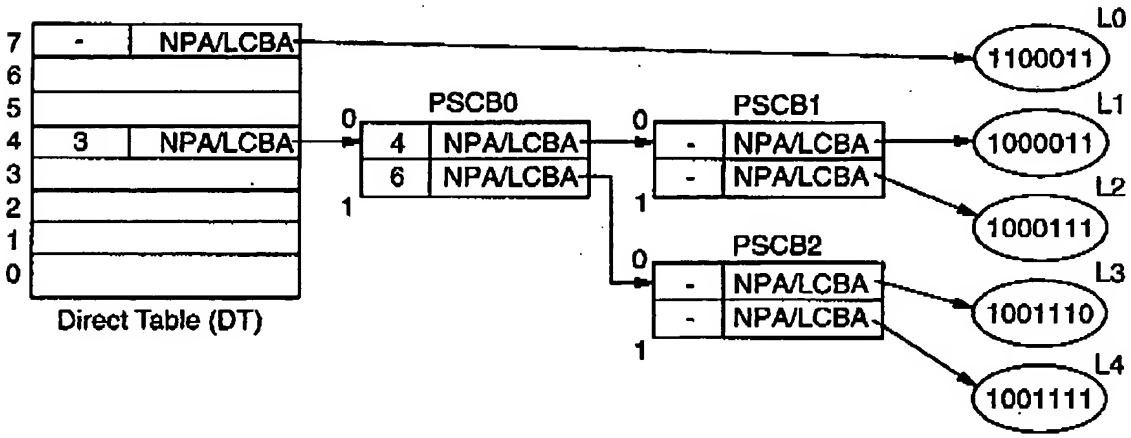


FIG. 10

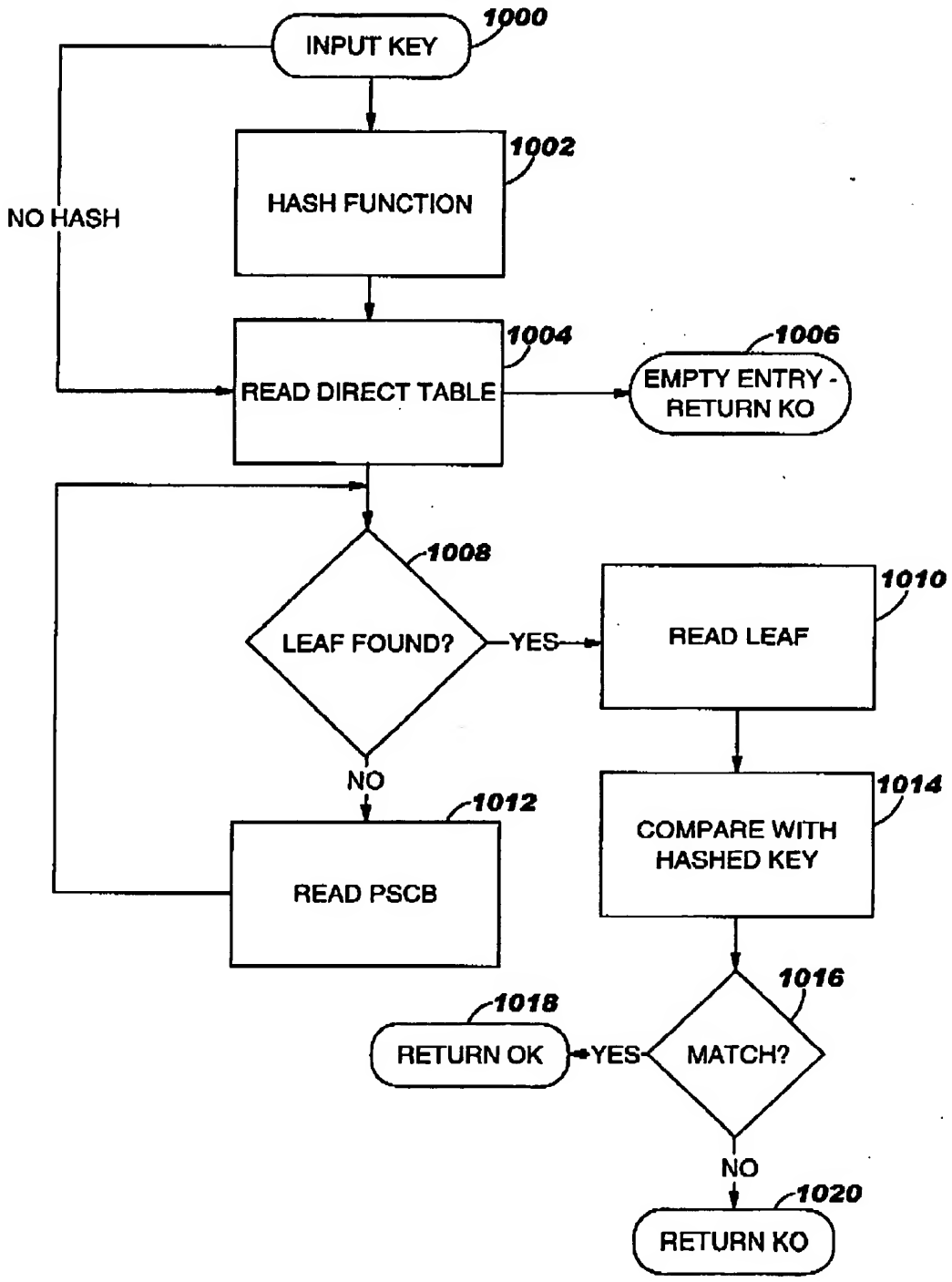

INPUT KEY
1000
HASH FUNCTION
1002
NO HASH
READ DIRECT TABLE
1004
EMPTY ENTRY - RETURN KO
1006
LEAF FOUND?
1008
YES
READ LEAF
1010
NO
READ PSCB
1012
COMPARE WITH HASHED KEY
1014
MATCH?
1016
YES
RETURN OK
1018
NO
RETURN KO
1020

FIG. 11

LUDefTable Tree Definition

Field	Size	Bits
CacheEntry	1	0
Tree_Type	2	2..1
hash-type	4	6..3
oolor_en	1	7
P1P2_max_size	5	12..8
NPARope_en	1	13
NPASMT_en	1	14
CompIndex_en	1	15
PSCB_fq_index	6	21..16
PSCB_Height	1	22
Mask_Vector_En	1	23
CompIndex	8	31..24
DT_base_addr	26	57..32
DT_size	4	61..58
DT_interleaf	2	63..62
Leaf_fq_index	6	69..64
Leaf_Width	2	71..70
Leaf_Height	3	74..72
DirectLeafEn	1	75

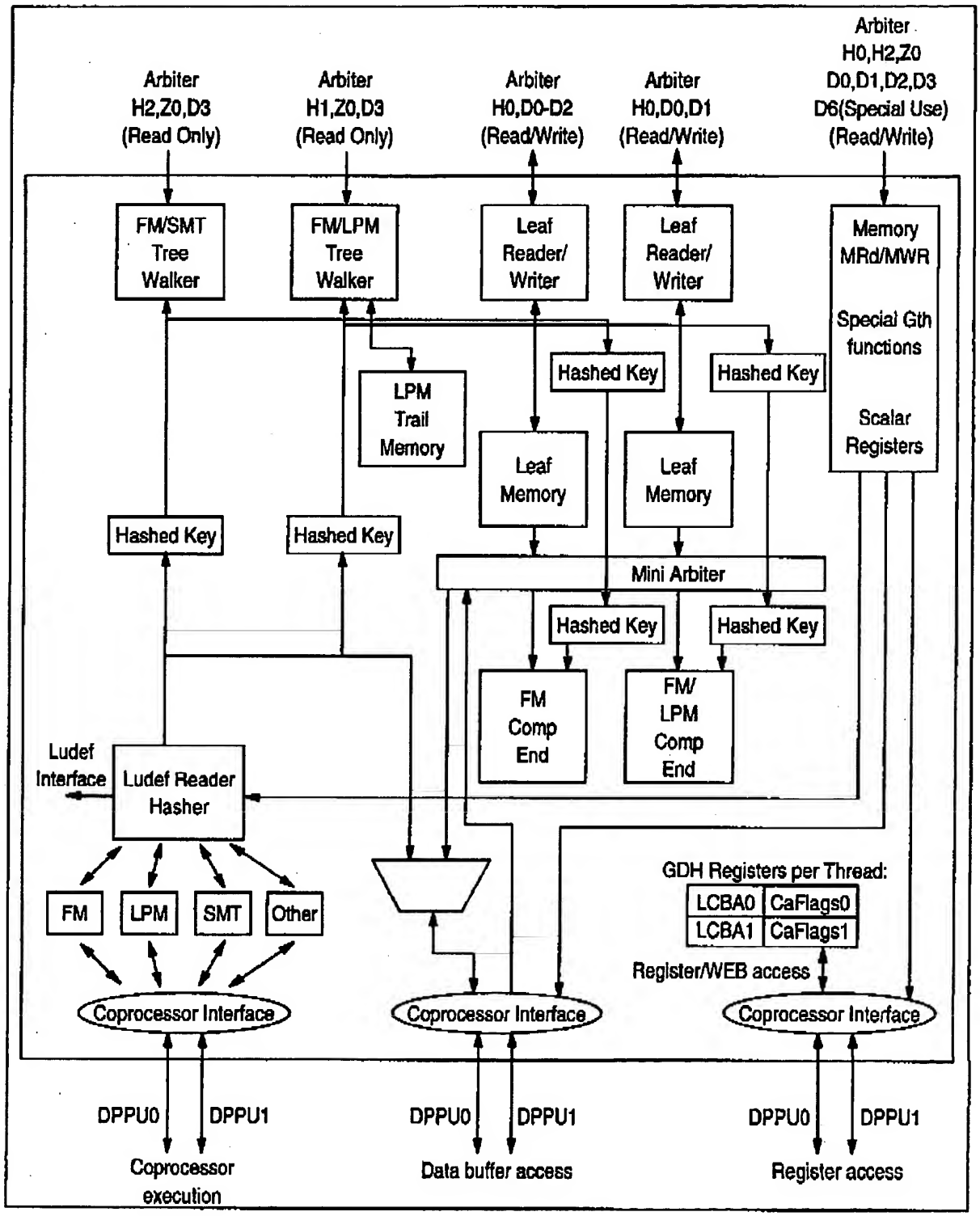
FIG. 12

Field	Size	Address in TSM where PSCB is located
NPA0	26	Next PSCB address: pointer to next PSCB in the tree for 0-part of PSCB
NBT0	8	Next bit to test for 0-part of PSCB
LCBA0	26	Leaf control block address: pointer to leaf for 0-part of PSCB
NPA1	26	Next PSCB address: pointer to next PSCB in the tree for 1-part of PSCB
NBT1	8	Next bit to test for 1-part of PSCB
LCBA1	26	Leaf control block addess: pointer to leaf for 1-part of PSCB
Index	8	Index of this PSCB (physically stored in the previous PSCB)
PatBit	1	The value of HashedKey[Index], based on the value of the Index field in the PSCB register

FIG. 13

Field Name	Length	Description
NLARope	4 bytes	Leaf chaining pointer, aging information and direct leaf information
Prefix_Len	1 byte	This field is not used by the TSE for FM trees and can be used by picocode
pattern	2 - 18 bytes	Pattern to be compared with the HashedKey
UserData	variable	The contents of this field is under complete picocode control; the UserData field can include one or more counters

FIG. 14


Arbiter H2,Z0,D3 (Read Only)
Arbiter H1,Z0,D3 (Read Only)
Arbiter H0,D0-D2 (Read/Write)
Arbiter H0,D0,D1 (Read/Write)
Arbiter H0,H2,Z0 D0,D1,D2,D3 D6(Special Use) (Read/Write)
FM/SMT Tree Walker
FM/LPM Tree Walker
Leaf Reader/ Writer
Leaf Reader/ Writer
Memory MRd/MWR
Special Gth functions
Scalar Registers
LPM Trail Memory
Hashed Key
Hashed Key
Leaf Memory
Leaf Memory
Hashed Key
Hashed Key
Mini Arbiter
Hashed Key
Hashed Key
FM Comp End
FM/ LPM Comp End
Ludef Interface
Ludef Reader Hasher
FM
LPM
SMT
Other
GDH Registers per Thread:
LCBA0
CaFlags0
LCBA1
CaFlags1
Register/WEB access
Coprocessor Interface
Coprocessor Interface
Coprocessor Interface
DPPU0
DPPU1
DPPU0
DPPU1
DPPU0
DPPU1
Coprocessor execution
Data buffer access
Register access